ABSTRACT

In a semiconductor integrated circuit device that includes macro cells (circuit blocks that can be designed independently) such as a storage circuit and operates synchronously with an external clock, total delay time from signal input to output is reduced and the speed of operation is increased. In the semiconductor integrated circuit device which has plural circuit blocks coupled in series for signal transmission and whose whole operation is controlled by a clock signal, the semiconductor integrated circuit device including first circuit blocks that receive input signals in response to a first timing signal based on a clock signal, and a second circuit block that forms output signals in response to a second timing signal based on the clock signal, a time difference between the first timing signal and the second timing signal is set to a non-integral multiple of the cycle of the clock signal.